QUASI-MONOLITHIC 4-GHz POWER AMPLIFIERS WITH 65-PERCENT POWER-ADDED EFFICIENCY*

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ABSTRACT

A highly miniaturized C-band 1-W GaAs FET amplifier, part of a three-stage power amplifier for communications satellite applications, has been designed, fabricated, and tested. It achieves a maximum power-added efficiency of 65 percent, and occupies an area of 0.20 x 0.36 in. The circuit employs a low-reactance termination at the second harmonic and low-loss quasi-monolithic circuitry. These results were obtained on the first fabrication run and with no circuit tuning.

INTRODUCTION

Active phased-array antennas require large numbers of power amplifiers which are small, lightweight, reliable, uniform, and efficient. Efficiency is an especially important characteristic because of its direct effect on DC power and heat removal requirements.

This paper describes the design and fabrication of a high-efficiency, single-stage C-band power amplifier. This amplifier is part of a three-stage, 30-dB gain, 2-W amplifier for the 3.7- to 4.2-GHz satellite band. The amplifier achieved a power-added efficiency of 65 percent on the first fabrication run and with no circuit tuning. To the authors' knowledge, this is the highest power-added efficiency reported for an FET amplifier above S-band. The high efficiency and small size result from:

(1) Class B (or "deep AB") operation
(2) Low-impedance reactive termination of the second harmonic at the drain
(3) The use of FETs selected on the basis of DC parameters
(4) The use of quasi-monolithic circuits to minimize the circuit losses and to achieve small size and uniformity

DC FET CHARACTERISTICS

The design for the 1-W amplifier was based on the Fujitsu FLK 202XV/106 FET. These FETs, nominally 1.5-W chip devices, were screened for low pinch-off voltage and high drain-to-gate breakdown voltage to maximize their output power and efficiency. The drain efficiency of an ideal FET operating in Class B mode is given by

$$\eta_d = \frac{\pi}{4}\left(\frac{1 - \alpha}{1 + \alpha}\right) \tag{1}$$

where

$$\alpha = \frac{V_K}{V_{BR} - 2V_{PO} - V_{BAR}}$$

and V_K = knee voltage
V_{BR} = drain-to-gate breakdown voltage
V_{PO} = pinch-off voltage
V_{BAR} = barrier potential.

All of the quantities in equation (1) are assumed to be positive. The drain efficiency approaches the theoretical maximum of 78.5 percent if V_{PO}, V_K, and V_{BAR} are small and V_{BR} is large. FETs with these characteristics and high gain are capable of high power-added efficiency.

SINGLE-ENDED CLASS B OPERATION

The advantages of Class B amplifiers over Class A amplifiers are well known. Aside from its higher efficiency, the ideal Class B amplifier consumes no power with zero input drive, whereas a Class A amplifier consumes constant power under all drive conditions. Under backoff, the efficiency of the Class B amplifier does not degrade as rapidly as that of the Class A amplifier.

The single-ended Class B amplifier, resistively terminated at all frequencies, generates a half-rectified sine wave given by the Fourier series

$$i(t) = \frac{1}{\pi} + \frac{1}{2}\sin(2\pi f_0 t) - \frac{2}{\pi}\sum_{n=2,4,\ldots}\frac{1}{n^2 - 1}\cos(2\pi n f_0 t) \tag{2}$$

Equation (2) shows that the waveform contains components at zero frequency (DC), the fundamental

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frequency, and the even harmonics. Further analysis shows that 84 percent of the total RF power delivered by a single-ended Class B amplifier is at the fundamental frequency, while 15 percent is at the second harmonic.

Snider [1] described the effect of various terminations at even and odd harmonics on both the efficiency and output power of ideal Class B amplifiers. He showed that the second harmonic must be terminated in a short circuit at the drain of the FET to prevent premature saturation and the dissipation of second harmonic power. Under these conditions, maximum output power and high efficiency are achieved at the fundamental frequency.

CIRCUIT DESIGN

The design for the amplifier was based on a combination of DC and small-signal RF measurements of the FET. From the small signal data, a lumped element equivalent circuit of the FET, shown in Figure 1, was derived. The input matching network was designed from the equivalent circuit, while the output circuit design was based on an FET model derived from both DC and small-signal RF measurements. The circuits employ a combination of lumped and distributed elements to achieve low loss and small size. A circuit schematic for the amplifier is shown in Figure 2.

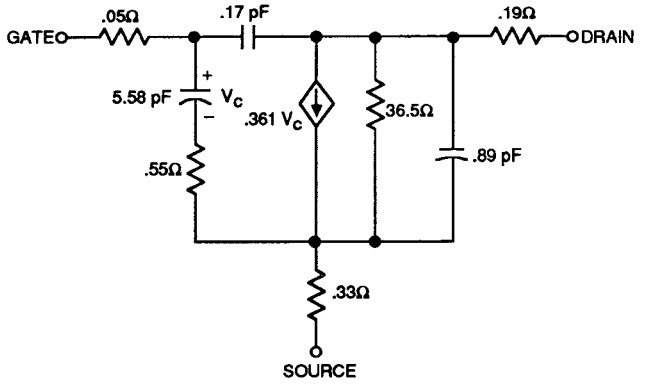

Figure 1. Small-Signal Model for the FET

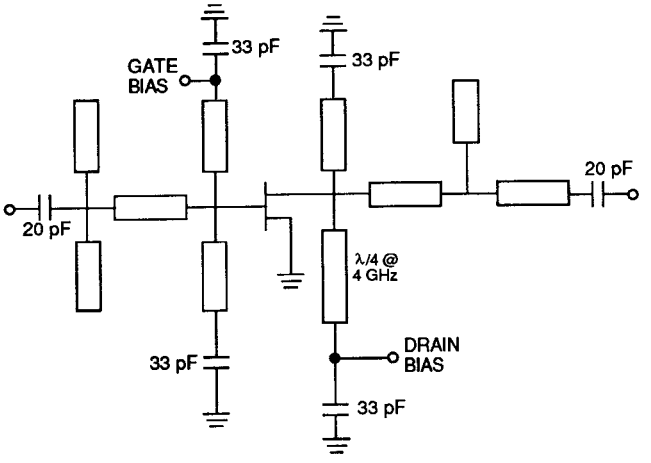

Figure 2. Circuit Schematic for the Amplifier

The first elements at the FET input are a pair of shunt inductors, resonant with the input capacitance of the FET at 4.2 GHz. Each inductor is connected to ground through a low-RF-impedance bypass capacitor. The next elements in the circuit, a series length of transmission line and an open-circuited stub, transform the parallel combination of the shunt inductors and FET input capacitance to 50 Ω. The last element in the network is a low-RF-impedance series DC-blocking capacitor. Gate bias is brought into the circuit via the top plate of one of the bypass capacitors and fed through the inductor to the FET.

The output matching network was designed to present the FET the load for maximum linear power, and also to terminate the second harmonic in a low reactance. A shunt stub at the drain terminal, one-quarter-wavelength long at the fundamental frequency and connected to ground through a low-RF-impedance capacitor, serves as the second harmonic termination. It is virtually transparent at the fundamental frequency. The other elements in the output matching circuit present the FET the load for maximum linear power at the fundamental frequency. A shunt inductor, resonant with the output capacitance of the FET at 4 GHz, is connected between the drain and a low-RF-impedance bypass capacitor. The remaining elements form a "T" network of transmission lines to transform the 50-Ω terminating impedance to the required load resistance value, computed from equation (3).

$$R_L^{CLassB} = \frac{V_{BR} - 2V_{PO} - V_{BAR} - V_K}{I_{MAX}} \qquad (3)$$

where I_{MAX} is the maximum current. For this device, V_{BR} = 17 V, V_K = 1 V, V_{BAR} = 0.6 V, V_{PO} = 1.5 V, and I_{MAX} = 800 mA, so the optimum load impedance is 15.5 Ω. Drain bias is brought into the circuit through the quarter-wave stub.

CIRCUIT FABRICATION

The amplifier was realized in a quasi-monolithic form, in which the passive circuits are fabricated monolithically on substrates separate from the FET. The circuits in the 1-W amplifier contain Si_3N_4 overlay capacitors, air bridges, and transmission lines. Other realizations could also incorporate thin film resistors and via-holes. The FET and matching circuits were subsequently combined on a common metal carrier, using conventional wire bond connections.

Because the networks are fabricated monolithically, quasi-monolithic circuits are smaller, less costly, easier to assemble, and more uniform than conventional hybrid MICs. In comparison to MMICs, and particularly with regard to power amplifiers, this technology has four main advantages. First, the matching networks can be fabricated on substrates of arbitrary thickness and dielectric constant to minimize circuit losses. Second, the FET can be made as thin as necessary to achieve low thermal resistance and permit better heat removal, resulting in improved reliability. Third, selected devices can be used,

resulting in better performance and higher yield. Finally, fabrication is easier and less costly than for MMICs.

RESULTS

A photograph of the assembled amplifier, which measures 0.36 x 0.20 in., is shown in Figure 3. Figure 4 shows plots of small-signal gain and input return loss of the amplifier under a Class AB bias (≈10 percent of I_{DSS}). The small-signal gain was 13.4 dB ± 0.3 dB in the 3.7- to 4.2-GHz band. The flat gain was achieved by mismatching the input of the FET at the low end of the band where the maximum available gain is high, and matching it at the upper end of the band.

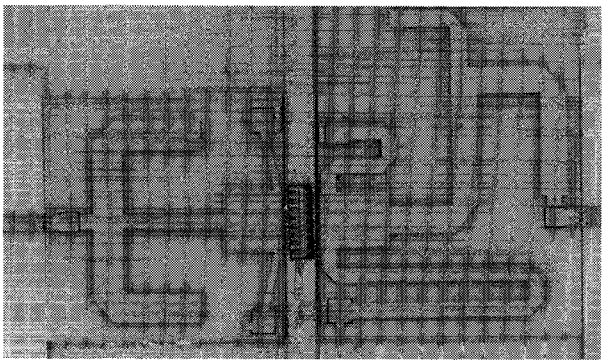

Figure 3. Photograph of the Amplifier

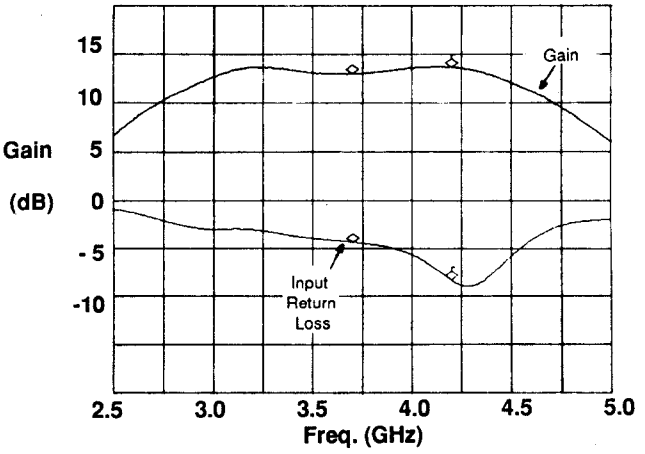

Figure 4. Plot of Small-Signal Gain and Return Loss vs Frequency

A plot of output power and power-added efficiency vs input drive at 4.1 GHz is shown in Figure 5. For an input drive level of 20 dBm, the measured output power and power-added efficiency were 30.4 dBm and 65.4 percent, respectively, corresponding to a drain efficiency of 71.5 percent. Figures 6 and 7 show plots of output power and efficiency as a function of frequency for several input power levels. For an input power of 19 dBm, the amplifier typically provides output power of 30.2 dBm, with a power-added efficiency of 58 percent across the 3.7- to 4.2-GHz band. Under 5-dB input backoff (14-dBm input) the amplifier is still quite efficient, delivering 27.5 dBm with 40-percent power-added efficiency.

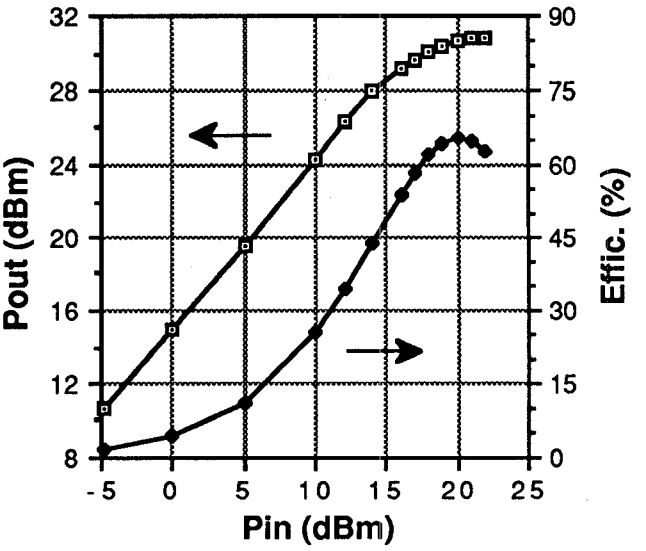

Figure 5. Plots of Output Power and Efficiency vs Input Drive

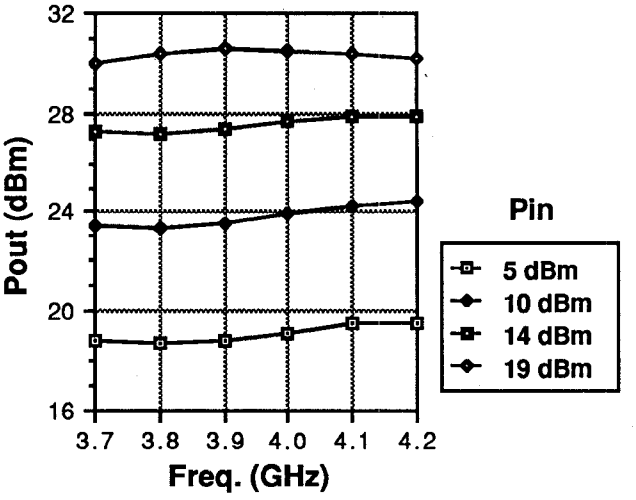

Figure 6. Plots of Output Power vs Frequency for Various Drive Levels

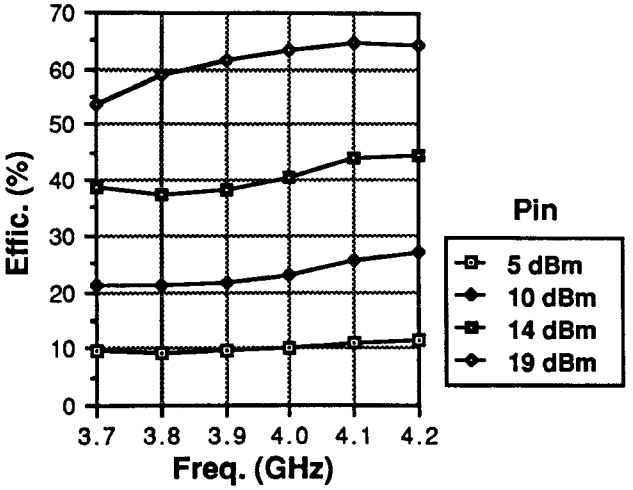

Figure 7. Plots of Efficiency vs Frequency for Various Drive Levels

Figure 8 shows that the dissipated power of the amplifier does not increase with backoff, as one would expect of a Class A amplifier. This characteristic has two important implications. First, good efficiency is preserved under backoff; and second, the thermal load is never higher than it is under full drive.

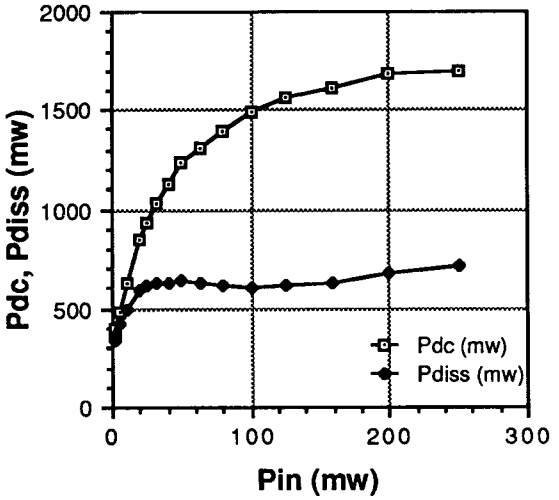

Figure 8. Plots of Supplied and Dissipated DC Power vs Drive Level

Third-order intermodulation distortion (IMD) and phase measurements at 4.2 GHz are shown in Figure 9. The transfer phase difference of the amplifier between low input drive and high input drive was 4.5°. The measured carrier-to-third-order intermodulation ratio (C/I_3) was 23 dB for a total two-tone input power of 19 dBm. As the input power was decreased, the third-order IMD decreased until it reached a minimum, beyond which there was no further improvement. This "bottoming" phenomenon arises because the device is biased near the virtual pinch-off voltage, where the V_{GS} - I_{DS} characteristic is nonlinear.

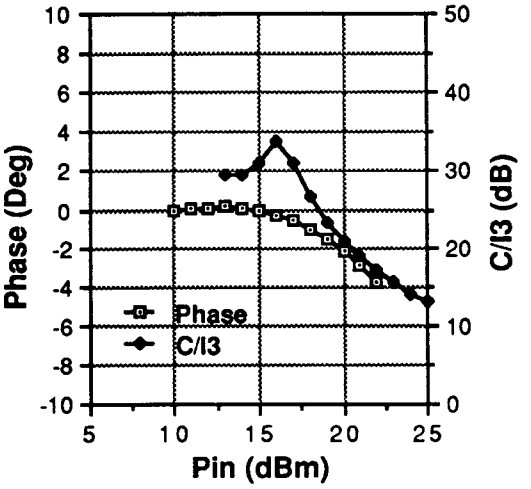

Figure 9. Plots of Phase and Third-Order IMD vs Drive Level

The 1-W amplifier was incorporated into the output stage of a three-stage, 30-dB gain, 2-W SSPA. Ten of these amplifiers, biased for linear operation, have been fabricated and tested. Maximum power-added efficiencies for the completed SSPAs range between 45 percent and 48 percent.

CONCLUSIONS

A highly miniaturized 1-W amplifier with a maximum power-added efficiency of 65 percent has been developed. The high efficiency is achieved by operating the amplifier in Class AB mode (≈10-percent I_{DSS}), terminating the second harmonic in a low reactance, using devices selected on the basis of DC parameters, and using quasi-monolithic circuits to minimize output circuit losses. IMD performance at intermediate and high drive levels was found to be comparable to that of a Class A amplifier.

ACKNOWLEDGMENTS

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